AMENDMENTS TO THE DRAWINGS:

The attached drawing sheet includes one (1) replacement sheet replacing original sheet 1, with amended Figure 1 and Figure 2.

Specifically, the drawings are objected to for not showing underlying chip wiring. The amendment to the drawings labels underlying chip wiring as 105 in Figure 1, as required by the Examiner. No new matter is added. Entry of the amendment is respectfully request.

REMARKS

Claims 1 – 5, 7 – 14 and 21 – 25 remain in the application and stand rejected. Claims 1, 8, 12, 14, 21 and 24 are amended herein. Claims 6 and 15 – 20 are previously canceled. No new matter is added by this amendment.

The drawings are objected to for not showing "'underlying chip wiring' with a terminal metal layer disposed on a chip passivating layer and connecting to underlying chip wiring through a via through said chip passivating layer … ." Responsive thereto, Figure 1 is amended on the enclosed replacement sheet. Specifically, the amendment to the drawings labels underlying chip wiring as 105 in Figure 1, as required by the Examiner. No new matter is added. Entry of the amendment is respectfully request.

The Specification also is amended to indicate in paragraph 0014 that label 105 identifies "underlying chip wiring" in Figure 1, as amended. Further, paragraph 0016 is amended for clarity in corresponding the description of forming the pads as described with reference to Figures 3A – H to the pad structure described with reference to Figure 1. Paragraph 0017 is amended to include a dash (-) indicating the hard test barrier layer thickness range. No new matter is added. Reconsideration and withdrawal of the objection to the drawings is respectfully requested.

Claim 8 is objected to for reciting "said diffusion barrier layer," which is asserted to lack antecedent basis. Responsive thereto, claim 8 is amended herein to recite "said adhesion/barrier layer … ." No new matter is added. Reconsideration and withdrawal of the objection to claim 8 is respectfully requested.

Claims 1, 2, 5, 7, 21, 22 and 25 are rejected under 35 U.S.C. §102(e) over U.S. No. 6,534,863 to Walker et al. Claims 3, 4, 8 – 14, 23 and 24 are rejected under 35 U.S.C. §103(a) over Walker et al., alone, in view of U.S. Patent No. 6,144,096 to

Lopatin., alone, or further in view of U.S. Patent No. 6,798,050 to Homma et al. and published U.S. application No. 2003/0034489 to Bhattacharya et al.

Applicants note that under 35 U.S.C. §103(c) the cited patent to Walker et al. is not a reference. Be that as it may, claims 1, 8, 14 and 21 are amended herein to indicate that the durable pads are probable without incurring probe damage. This is supported by the specification as filed and, in particular by paragraphs 0002 – 8 and 0018. No new matter is added.

Further, Walker et al. teaches forming a feature 21 in a dielectric layer and a "layer 22 of **liner** material may be deposited on the entire surface of the substrate 20, including the **sidewalls and bottom** of feature 21." Col. 4, lines 29 – 32 (emphasis added). Thus, the feature 21 size, pitch and spacing are all controlled by second or third order parameters, e.g., dielectric material, dielectric etchant, dielectric etch rates, dielectric thickness, etc. For a typical wet etch, adjacent features 21 can be formed no closer than twice the dielectric thickness. Otherwise, the dielectric between liners would etch away. Further, adjacent liners have parallel sidewalls the entire depth of the feature 21 that results in pad to pad capacitance. This capacitance not only loads the I/Os, but introduces cross talk. Moreover, Walker et al. fills this liner 22 with a seed layer 23, a first electroplated layer 24 and completes the plug with a "second electroplated layer 26 is formed over the first electroplated layer 24, which will serve as the pad for the common I/O site." Col. 4, lines 38 – 57 and col. 5, lines 1 – 3. So, there is no pad until Walker et al. forms the second electroplated layer 26.

Therefore, Walker et al. fails to teach or suggest a conducting layer pad, a hard test barrier layer on the pad and a plate passivating layer on the hard test barrier layer as the claims recite, to allow "finer C4 pitch, e.g., 3 mil bumps and smaller." Paragraph 0018. Therefore also, Walker et al. fails to teach or suggest the present invention. Reconsideration and withdrawal of the rejection of claims 1 – 5, 7 – 14 and 21 – 25 under

35 U.S.C. §§102(e) and 103(a) over Walker et al., alone or further in combination with any other reference of record, is respectfully requested.

The applicants thank the Examiner for efforts, both past and present, in examining the application. Believing the application to be in condition for allowance, both for the amendment to the claims and for the reasons set forth above, the applicants respectfully request that the Examiner reconsider and withdraw the objection to claim 8, reconsider and withdraw the rejection of claims 1 – 5, 7 – 14, and 21 – 25 under 35 U.S.C. §§102(e) and 103(a), and allow the application to issue.

As previously noted, the applicants believe that the matter presented in the written description of the present application is quite different than, and not suggested by, any reference of record. Accordingly, should the Examiner believe anything further may be required, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below for a telephonic or personal interview to discuss any other changes.

Please charge any deficiencies in fees and credit any overpayment of fees to IBM Corporation Deposit Account No. 09-0458 and advise us accordingly.

Respectfully Submitted,

April 15, 2008
(Date)

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APPENDIX